Lab 3
Introduction to VHDL

Objectives

- To get familiar with the Xilinx VHDL Editor Tool.
- To design and implement simple combinational logic circuits using VHDL at the Behavioral and Structural levels.
- Synthesize, simulate and test combinational circuits.
- To download your circuit onto the prototype board and test it.

Laboratory Instructions

- Use the Xilinx VHDL editor to create the VHDL source file(s) for your design before coming to the lab.
- Create a directory with your name on drive C of your lab PC. Use this directory to create your project, store your results, bitsteams, etc. during the lab session.
- You can bring a complete project (i.e. *project.pdf* file and *project* directory) on a floppy disk and then use the **Copy Project** command from the Project Manager menu to copy it into the directory you created above.
- Alternatively, you create a new project in your directory on the C drive and then copy your VHDL to that new project directory. Remember to *Add* your VHDL file to the project.
- Refer to appendix C on how to create a project, enter the VHDL code, and synthesize the VHDL code to a netlist.
- Perform functional simulation of your design and have it checked by your TA.
- If the circuit works as expected, implement it using the prototyping board assigned to you.
- Use keyboard and LEDs available to apply input stimuli and observe the outputs. Disconnect the XSPORT (parallel port) when you apply input stimulus from the workbench.
- Test and demonstrate your circuit to your TA.

Design Problems

Using the Xilinx VHDL Editor, design, test and demonstrate the following circuits.

1. Design the full adder using VHDL at the Behavioral level.
2. Design the full subtractor using VHDL at the Behavioral level.
3. Design the full adder using VHDL at the Structural level.
4. Design the full subtractor using VHDL at the Structural level.
5. Design a 4-to-1 multiplexer using VHDL at the Behavioral level as a module that can be used later as a building block for other circuits.